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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/866,424	05/25/2001	Nobushige Moriwaki	36856.502	5983

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EXAMINER

DINH, TUAN T

ART UNIT PAPER NUMBER

2827

DATE MAILED: 08/20/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No.	Applicant(s)
	09/866,424	MORIWAKI ET AL.
Examiner	Art Unit	
Tuan T Dinh	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

1) Responsive to communication(s) filed on 25 May 2001.

2a) This action is **FINAL**.                            2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

4) Claim(s) 1-20 is/are pending in the application.

4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.

5) Claim(s) \_\_\_\_\_ is/are allowed.

6) Claim(s) 1-20 is/are rejected.

7) Claim(s) \_\_\_\_\_ is/are objected to.

8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on 25 May 2001 is/are: a) accepted or b) objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) The proposed drawing correction filed on \_\_\_\_\_ is: a) approved b) disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) The oath or declaration is objected to by the Examiner.

#### Priority under 35 U.S.C. §§ 119 and 120

13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All b) Some \* c) None of:

1. Certified copies of the priority documents have been received.

2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.

3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) The translation of the foreign language provisional application has been received.

15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

#### Attachment(s)

1) Notice of References Cited (PTO-892)

2) Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) Information Disclosure Statement(s) (PTO-1449) Paper No(s) 5.

4) Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_.

5) Notice of Informal Patent Application (PTO-152)

6) Other: \_\_\_\_\_.

## DETAILED ACTION

### *Drawings*

1. The informal drawings are not of sufficient quality to permit examination.

Accordingly, new drawings are required in reply to this Office action.

The formal is required of sufficient quality without Japanese characters

Figure 6 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the switching module, in which does not any switches as function as the switching module" must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

### *Claim Rejections - 35 USC § 112*

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claims 1, line 3, it is confuse. Based on the drawings in this application, does applicant mean “a plurality of ceramic capacitors”, which is a plurality of chip-ceramic capacitors?”

Regarding claim 1, lines 3-4, it is unclear. Does applicant mean of “a plurality of capacitors provided on a top surface of each of substrates?”

Regarding claim 1, lines 5-10, it is unclear. The phrase of “first and second feeding unit lands...connected to each other” is not understood. Does applicant mean “...unit lands...arranged on both surfaces of each substrate?”. Also, what does applicant mean “the first and second feeding unit lands disposed on both surfaces of the substrates being electrical connected each other?”

Regarding claim 1, lines 11-17, is in unclear. The phrase of “a conductive spacer inserted between said substrates...overlying one of the substrates” is not understood. Does applicant mean “a plurality of conductive spacers” inserted between each of said substrates?”

Regarding claims 3 and 13, lines 5-8, it is unclear. The phrase of “the first feeding unit landss... said plurality of substrates, respectively” is not understood

Regarding claims 11, line 4, it is confuse. Based on the drawings in this application, does applicant mean “a plurality of ceramic capacitors”, which is a plurality of chip-ceramic capacitors?”

Regarding claim 11, lines 4-5, it is unclear. Does applicant mean of "a plurality of capacitors provided on a top surface of each of substrates?"

Regarding claim 1,1 lines 5-10, it is unclear. The phrase of "first and second feeding unit lands...connected to each other" is not understood. Does applicant mean "...unit lands...arranged on both surfaces of each substrate?". Also, what does applicant mean of "the first and second feeding unit lands disposed on both surfaces of the substrates being electrical connected each other?"

Regarding claim 11, lines 12-18, is in unclear. The phrase of "a conductive spacer inserted between said substrates...overlying one of the substrates" is not understood. Does applicant mean "a plurality of conductive spacers" inserted between each of said substrates?"

#### ***Claim Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sobhani et al. (U. S. Patent 5,481,134) in view of Inoguchi (U. S. Patent 6,185,105).

As best understood to claims 1, 8, 11, and 18, Sobhani discloses stacked high density interconnected integrated circuit system (10-figure 1, column 3, line 11) capable

of being an inverter comprising an inverter capacitor module as shown in figures 1-6 comprising:

a plurality of substrates (40, column 3, line 24) including:

a plurality of conductive spacers (20, column 3, line 23) inserted between each of said plurality of substrates;

a fixing element (12, 14, column 3, lines 15-20) arranged to fix said plurality of substrates laminated said conductive spacer; and

a motherboard (11, column 3, line 15) capable of being a switching module that is fixed below a bottom substrate among said plurality of substrates (see figure 1) that are laminated; wherein said switching module is fixed to said plurality of substrates by said fixing element.

Sobhani does not disclose a plurality of ceramic capacitors provided on a top surface of each of said substrates; and each of substrate having first and second feeding unit lands having conductive films laminated on both surfaces of the substrate.

Inoguchi shows a circuit board (substrate 1-figure 2) comprising a plurality of ceramic capacitor (see figure 2) mounted on a top surface of the circuit board, the circuit board having first and second conductive films (11, 12) laminated on both surfaces of the circuit board (1).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have a substrate having film layers laminated on both surfaces of the substrate and having a plurality of capacitors mounted on a top surface of the

substrate as taught by Inoguchi to employ the inverter capacitor module of Sobhani in order to prevent a static electricity in high impedance circuit.

As to claims 2, 12, Inoguchi shows the plurality of ceramic capacitors each includes first and second terminals and the first terminal is electrically connected to the first feeding unit land and the second terminal is electrically connected to the second feeding unit land.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have terminals of the capacitor connected to the first and second lands as taught by Inoguchi to employ the inverter capacitor module of Sobhani in order to provide electrical connections of components to the circuit board.

As best understood to claims 3 and 13, Sobhani discloses the module as shown in figures 1-6 plurality of substrates (40) each includes a printed-circuit board and first and second through-hole electrodes (44-figure 3a) arranged to establish electrical connections

As to claims 4 and 14, Sobhani discloses the module as shown in figures 1-6 further comprising:

a projecting unit (rods 12) arranged to upwardly project from the top surface or downwardly project from the bottom surface of said conductive spacers (20) and including a male screw (14, column 3, line 20) disposed on the outer periphery thereof;

a hole (21) including a female thread (rod 12) capable of being engaged with said male screw (14) in the inner periphery thereof and provided in the bottom surface or the top surface of said conductive spacer; and

a plurality of conductive spacers (20) are fastened via said male screw and said female thread provided in said hole.

As to claims 5 and 15, Sobhani discloses all of the limitations of the claimed invention, except said plurality of ceramic capacitors each includes first and second lead terminals each having different polarities and including a plurality of metal-tongue pieces.

Inoguchi shows capacitor components disclosed in figures 2-3 having first and second lead terminals (15a, 15b) each having different polarities.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to use component having polarities terminals as taught by Inoguchi to employ the module of Sobhani in order to provide a correction connection of the components mounted on a circuit board without causing short circuit.

As to claims 6-7, and 16-17, Inoguchi shows an insulating coatings (13, 14) are disposed on both surfaces of the conductive films of the first and second feeding units.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to use insulating coatings disposed on the surface of the conductive films as taught by Inoguchi to employ the module of Sobhani in order to provide a thermo-mechanical stress on the circuit board.

As to claims 9-10, and 19-20, Sobhani discloses the module as shown in figures 1-6 wherein the fixing element further includes a plurality of through holes (44) formed in the plurality of substrates (40) and arranged to receive the plurality of bolts (14).

***Conclusion***

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Ameen et al. and Moden et al. disclose related art.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan T Dinh whose telephone number is 703-306-5856. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L. Talbott can be reached on 703-305-9883. The fax phone numbers for the organization where this application or proceeding is assigned are 703-305-1341 for regular communications and 703-305-1341 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

TD  
August 12, 2002.

*Albert W. Paladini 8-12-02*  
ALBERT W. PALADINI  
PRIMARY EXAMINER